Claims

What is claimed is:

1. A method of forming a semiconductor structure comprising the steps of:
a) providing a semiconductor substrate;
b) providing a layer of SiGe over at least a region of the semiconductor substrate;
c) providing a mesa of over a portion of the SiGe layer;
d) depositing a polycrystalline silicon layer over the mesa and over lower adjacent regions of the SiGe layer;
e) planarizing the polycrystalline silicon layer to expose the mesa and,
f) etching the mesa to expose a region of SiGe below.

2. A method as defined in claim 1, wherein the mesa is a SiO_xN_y material.

3. A method as defined in claim 1, wherein step (e) is performed by polishing the polycrystalline silicon layer.

4. A method as defined in claim 3, wherein the polishing is performed to expose a surface of the mesa.

5. A method as defined in claim 1, wherein the step of etching etches away the mesa while substantially preserving the adjacent polysilicon SiGe layers.

6. A method of forming a semiconductor structure comprising the steps of:
a) providing a substrate of a first semiconductor type;
b) providing a second layer of a second type of semiconductor material over at least a region of the first semiconductor substrate;
c) providing a mesa over a portion of the second layer, the mesa being a material that can bond to the second type of semiconductor and that can be etched by an etching source without etching the second type of semiconductor;

d) depositing a conductive layer over the mesa and over lower regions adjacent the mesa that will not be etched by the etching source;

e) planarizing the conductive layer; and,

f) etching the mesa to expose a region of the second layer below.

7. A method as defined in claim 6, wherein the first semiconductor type is has a conductivity of a first type, and wherein the second layer of the second type of semiconductor material has a second conductivity type.

8. A method of forming a semiconductor structure comprising the steps of:

a) providing a semiconductor substrate;

b) providing a layer of SiGe over at least a region of the semiconductor substrate;

c) providing a mesa over a portion of the SiGe layer;

d) depositing a polycrystalline silicon layer over the mesa and over lower adjacent regions of the SiGe layer;

e) exposing an upper surface of the mesa by removing the polycrystalline silicon layer over the mesa; and,

f) removing the mesa to expose a region of SiGe below.

9. A method as defined in claim 8, wherein the mesa is removed by an etching process.

10. A semiconductor device comprising:

a silicon substrate forming one of a collector and an emitter, the substrate being of a first conductivity type;

a layer of SiGe of a second conductivity type covering at least a portion of the silicon substrate; and,

a first layer of polysilicon of the second conductivity type at least substantially supported by and covering a substantial portion of the SiGe layer with the exception of a window region, forming a SiGe base of the transistor; and, a second layer of polysilicon of the first conductivity type covering and contacting the SiGe base of the transistor, said layer of polysilicon forming the other of the collector and the emitter.

11. A semiconductor device as defined in claim 10 wherein the silicon substrate is n-type material and forms the collector.

12. A semiconductor device as defined in claim 11 wherein the layer of SiGe is p-type material, and wherein the second layer of polysilicon is n-type material and forms the emitter.

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13. A semiconductor device comprising:
a silicon layer of a first conductivity type;
a layer of SiGe of a second conductivity type covering at least a region of the silicon layer; and,
a first layer of polysilicon of the second conductivity type at least substantially supported by and covering a substantial portion of the SiGe layer with the exception of a small window; and, a second layer of polysilicon of the first conductivity type covering the window and contacting the SiGe layer.

14. A semiconductor device as defined in claim 13, wherein the silicon layer serves as a substrate and is substantially thicker than the layer of SiGe.

15. A semiconductor device as defined in claim 13 wherein the SiGe layer has a substantially uniform thickness.

16. A semiconductor device as defined in claim 13 wherein the thickness of the SiGe layer covered by the second layer of polysilicon is of a substantially a same thickness and impurity concentration as the remaining portion of the layer of SiGe covering at least a region of the silicon layer.

17. A method of applying a semiconductor seed layer to a mixed topology substrate having regions of exposed semiconductor material and regions of exposed dielectric material, comprising the steps of:

disposing the substrate in a growth chamber and nucleating the seed layer by exposing the semiconductor material and dielectric material to an atmosphere of gases, the gases being presented at a predetermined flow rate, temperature and pressure, wherein the temperature is less than 600 °C, the pressure is less than 10^{-2} mbar, and the flow rate is less than 5 sccm.

18. A method as defined in claim 17 further comprising the step of cleaning surfaces of the substrate for removal of contamination and debris.

19. A method as defined in claim 17 wherein at least one of the gases is hydrogen and has a flow rate of less than 500 sccm and wherein another of the gases is silane and has a reduced flow rate of less than 20 sccm and wherein said gases are injected into the deposition chamber to initiate the nucleation of silicon and produce the seed layer on all exposed surfaces.

20. A method as defined in claim 17, wherein the seed layer is deposited to have a thickness of between 2 to 20nm.

21. A method as defined in claim 17 wherein the seed layer is doped with impurities.